A Survey on Results of Coding for Fault Tolerant Parallel Filters

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Abstract – Trustworthiness of mission critical systems is a weighty criterion for any system and is achieved by appropriate fault detection techniques. Digital filters are most often integrated in modern digital signal processing systems for the processing of signals. According to Moore's law, number of integrated circuits used in signal processing as well as communication systems are becoming more circuitous and their productions are doubling, per year. This triggered the need for fault tolerant executions. This paper replaces the conventional Error Correction Code based protection scheme to an efficient coding scheme for making the Digital FIR filters fault tolerant with less number of redundant filters and to improve the performance of the filters. Fault tolerance requires hardware redundancy and all the existing systems uses redundant modules for that. For any number of filters number of redundant modules will be least in the proposed technique.

Index Terms – Soft Errors, Single Event Upsets and Single Event transients, Efficient Coding Scheme, FIR filter, Redundancy.

1. INTRODUCTION

As the number of devices per chip and system performance has been improving exponentially, the complexity of electronic circuits has also increased. In space, medical, security and automotive applications which need crucial reliability, presence of electronic circuits are plentiful. The Moore's law states that the number of transistors in a dense integrated circuit approximately doubles every two years. This increased intricacy makes the circuit more vulnerable to errors. Manufacturing variations and soft errors are the major reliability challenges. Undesired outputs are mainly due to soft errors. It is the temporary state or transition which inverses the original state of the system.

If any high energy particle hits a circuit node the energy gets transferred to the circuit node, which results in spurious transition and can change the logical value of a circuit node by creating a temporary error that can affect the system operation. Silicon on Insulator (SOI) which is a special manufacturing process was used to protect the circuits. Major breakthrough for protection of the circuits was the ideology to add redundancy.

2. RELATED WORK

Triple Modular Redundancy (TMR) is the most accustomed technique which makes design three fold the system and adds voting logic to correct errors. It is the best example of a technology which uses the concept of redundancy. Redundant modules are additional systems which are used to protect the desired system. As it triples the area and power of the circuit, it is not acceptable in some applications. Another method [4] is to use the algorithmic properties of the circuit to detect or correct errors which can reduce the overhead required to protect the circuit. This is referred to as Algorithm-Based Fault Tolerance (ABFT). Over the years as the technology has been scaled from about 1300nm to about 10 nm technology, large number of transistors are integrated on a single chip. Complex signal processing applications and biomedical applications uses parallel digital filters for the processing of large number of filters. In this paper most efficient protection scheme with minimal hardware utilization is explored by replacing multipliers with shifters.

For many applications signal processing circuits are well suited. These circuits mainly include parallel digital FIR filters. FIR filters are most often chosen over IIR filters as they have regular structures and are stable at linear phase. Over the years many ABFT techniques [3] have been proposed to protect the basic blocks that are commonly used in those circuits. Parseval theorem [4] was one of the most basic algorithms used to check the error rate in a system.In [5] mitigation of soft errors were the main concern and there various technologies were proposed like self-checking design, Error masking design , error trapping design which was based on Muller C element. Then shim came with the concept of Algorithmic soft error tolerance. Three distinct techniques were proposed [6] and compared their protection efficiency. The Fine Grain Soft Error Tolerance and Sub word Detection processing schemes were explored in [7] which exploits the concept of logic masking. In bridging concurrent and noncurrent error detection multipliers are replaced by constant shifting [8] this idea was explored to make a new scheme for protection .An arbitrary matrix designed [2] to protect the

parallel filters with less number of redundant modules was also used in this scheme.

3. FILTERS ARRANGED IN PARALLEL

Computers and computer applications use digital signals so they most often use parallel digital filters for their processing. A digital filter can be realized with an FIR filter or an IIR filter implementation. FIR filters are most commonly used because it has high stability. This work addresses an efficient fault tolerance technique to protect configurations of parallel FIR filters. FIR filter can be implemented using the following equation.

$$y[\mathrm{n}] = \sum_{l=0}^{N}(x[n-l].h[l]) \qquad (1)$$

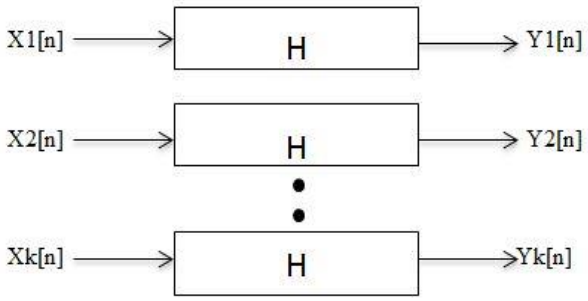

Figure 1: Parallel filters with same response

Where x[n] is the input signal, y[n] is the output signal and h[l] is the impulse response of the filter. N is the order of the filter. Order represents the number of delay elements used in the filter. Linearity property is the most important property of digital filters which is exploited in this scheme. It states that sum of any combination of the outputs can be obtained by adding corresponding inputs and filtering the inputs with the same impulse response of the filter. It is explained in equation (2)

$$Y1[\mathrm{n}] + Y2[n] = \sum_{l=0}^{\infty}((\mathrm{X1[n-l]} + \mathrm{X2[n-l]}).\mathrm{h[l]}) \qquad (2)$$

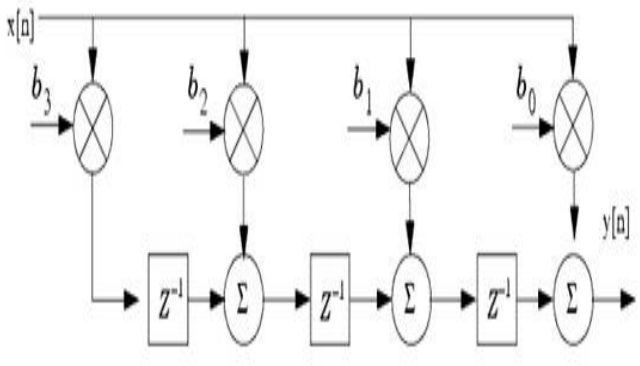

Fig 2 : Transpose form implementation of FIR filter

The FIR filter can be implemented with direct form or tanspose form realization. The proposed technique addresses transposed form implementation and the simple observations shown in (2).

4. EXISTING SCHEME

The protection of parallel filters was done using Error Correction Codes basically hamming code.

Information Bits	Parity Bits
4	3
8	4
12	5
27	6

Table I: Relation between information bits and parity bits.

Hamming codes are mainly used to locate whether any transmitted bit is in error and to correct it, so that error free bits are received at the receiver. To protect information bits to be transmitted from errors Hamming codes transmit some number of parity bits along with the information bits. The number of parity bits to be added is based on the Hamming rule.

$$r + p + 1 \geq 2^{p} \qquad (3)$$

So according to these observations to protect four information bits from errors three parity bits have to be added. It is explained in Table 1.With the same concept of hamming codes erroneous outputs and faulty filter can be corrected.

Filters to be protected	Redundant Filters
4	2
8	2
12	2
27	2

Table II: Relation between Filters to be protected and filters added as redundant filters for Fault tolerance

Here in the conventional scheme inputs are represented as X1, X2, X3, and X4 these are processed through filters F1, F2, F3, F4, F5, F6 and F7 with same response arranged in parallel. Considering equation1 and figure2 the responses of the given inputs are Y1, Y2, Y3, and Y4. For example

$$\mathrm{Y1}=\sum_{l=0}^{N}(x1 \cdot h[l]) \qquad (4)$$

Inputs to the redundant filters were coded according to the hamming codes and its response is given as

Q1 [n] = $\sum_{l=0}^{N}(x1 + x2 + x3)h[l])$ (5)

S1	S2	S3	Faulty Output	Action
0	0	0	None	None
1	1	1	Y1	Correct F1
1	1	0	Y2	Correct F2
1	0	1	Y3	Correct F3
0	1	1	Y4	Correct F4
1	0	0	Q1	Correct F5
0	1	0	Q2	Correct F6
0	0	1	Q3	Correct F7

Table III: Realization of Conventional Scheme for Fault tolerance

Where Q1[n] is the output of the first redundant filter and similarly Q2[n] and Q3[n]. These equations of the output of the redundant filters are taken to check whether there is any error in the output or to find any faulty filter, that is expressed as

Q1 [n] = Y1+Y2+Y3 (6)

Equations 5 and 6 are then equated and checked for equality. Similarly Q2 [n] and Q3[n] are also equated to corresponding sum of outputs. Thus there are three sets of equations which were expressed as

Q2 [n] = Y1+Y2+Y4 (7)

Q3 [n] = Y1+Y3+Y4 (8)

Now these equations 6, 7 and eight have been checked for equality and if all the three were not pleasant the equations then first filter is misguided so to produce an undesired output. And if 6 and 7 are usually not satisfied then filter 2 is erroneous. Filter 3 is inaccurate if 6 and eight will not be gratified. After finding the faulty filter we correct it with the aid of reconstructing the outputs. The reconstructed outputs are:

Y_{c1} [n] = Q1 [n] − Y2− Y3. (9)

Y_{C2} [n] = Q2 [n] − Y1 − Y4. (10)

Y_{C3} [n] = Q3 [n] − Y1 − Y4. (11)

Y_{C4} [n] = Q2 [n] − Y1 − Y2. (12)

5. PROPOSED SCHEME

In order to reduce the number of redundant filters to be added to protect original filters an efficient coding scheme is proposed. The main advantage of this scheme is expressed in Figure3. Here the need for redundant modules to protect the original modules is minimized

Let us first consider a four parallel filter to be protected from errors. With efficient coding concept number of redundant modules to be added is minimized to two. . The main concept behind this scheme is substituting the bits by numbers, and each filter is represented by a number. An Arbitrary matrix was designed:

$$A = \begin{matrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & a_{33} & a_{34} \\ a_{41} & a_{42} & a_{43} & a_{44} \\ a_{51} & a_{52} & a_{53} & a_{54} \\ a_{61} & a_{62} & a_{63} & a_{64} \end{matrix}$$

First four rows of the matrix forms an identity matrix in order to make the same input to pass through. The inputs to the redundant filters are a combination of other filters input. In order to make it simple all the elements of fifth row was given as one and the sixth row as 1, 2, 4 and 8. The arbitrary matrix used in this scheme is given by:

$$A = \begin{matrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 2 & 4 & 8 \end{matrix}$$

So the inputs are given as:

$$x_5[n] = x_1[n] + x_2[n] + x_3[n] + x_4[n] \quad (13)$$

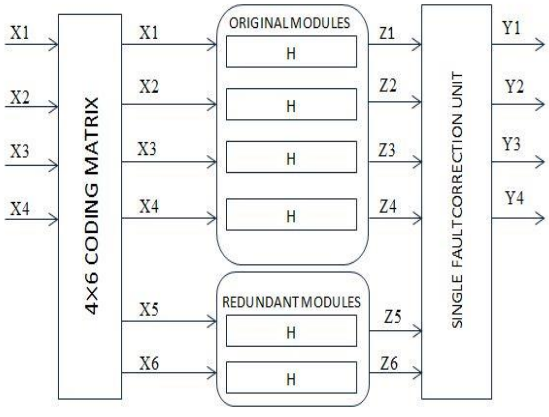

Figure 3: Block Diagram of Proposed Scheme

$$x_6[n] = x_1[n] + 2x_2[n] + 4x_3[n] + 8x_4[n] \quad (14)$$

The corresponding outputs of the redundant filters according to linearity property are given as:

$$Z_5[n] = \sum_{l=0}^{\infty}((x_1[n-l] + x_2[n-l] + x_3[n-l] + x_4[n-l]).h[l]) \quad (15)$$

$$Z_6[n] = \sum_{l=0}^{\infty}((x_1[n-l] + 2x_2[n-l] + 4x_3[n-l] + 8x_4[n-l]).h[l]) \quad (16)$$

Here for locating the erroneous filter first there is a need for checking whether the linearity property is satisfied for that the left hand side and right hand side of equation (8) and (9) are analysed. Two check registers were assigned.

$$P1 = Z_5 - (Z_1 + Z_2 + Z_3 + Z_4) \quad (17)$$

$$P2 = Z_6 - (Z_1 + 2Z_2 + 4Z_3 + 8Z_4) \quad (18)$$

Four error correction registers were assigned to locate the erroneous filter, which are given as e_1, e_2, e_3 and e_4. In this scheme twelve multipliers, three for input x_6, three for its corresponding output y_6, three for check register and three for the error correction register. In this proposed scheme all these multipliers are replaced by shifters. Binary multiplication is replaced here using left shift logic.

e1	e2	e3	e4	Faulty Output	Action
0	0	0	0	None	None
0	#	#	#	Z1	Correct F1
#	0	#	#	Z2	Correct F2
#	#	0	#	Z3	Correct F3
#	#	#	0	Z4	Correct F4
#	#	#	#	Z5	Correct F5
#	#	#	#	Z6	Correct F6

Table IV: Realization of Proposed Scheme for Fault tolerance

6. RESULTS AND DISCUSSION

Results and discussion mainly includes the behavioural simulation and RTL schematic implementation of the design. RTL schematic describes the logic utilization in a FPGA and In this scheme RTL schematic is shown in fig 4.Here four parallel digital FIR filters are protected using an efficient coding scheme and the multipliers are replaced with shifters. The binary left shift is utilized here. When a study was conducted to look whether there is any change when the bit width increases, it was found that when the bit width increases the number of Look up tables, flip-flops, DSP48 tiles etc, increases.

Here we can see that as the number of redundant filters increases the area utilized also increases. In the simulation result X1 is represented by Xin1 and similarly others.

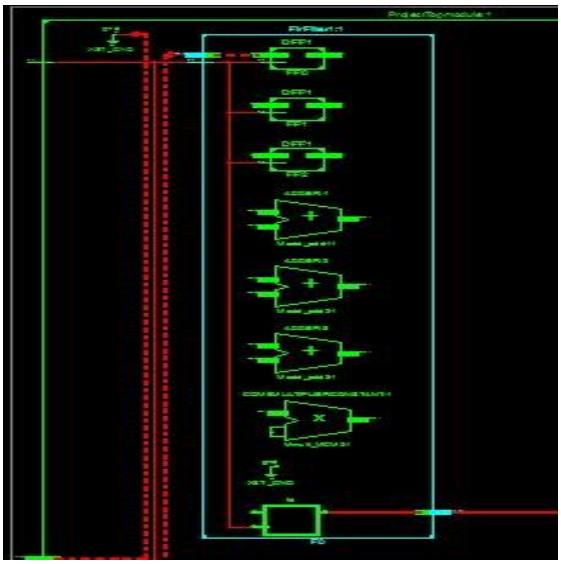

Fig4: Resources in a Single Filter

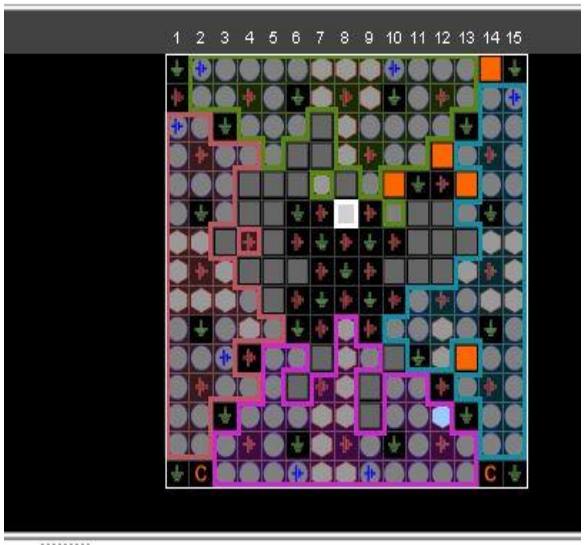

Fig5: Input Output Pin Diagram of Proposed Scheme Using Xilinx Plan Ahead

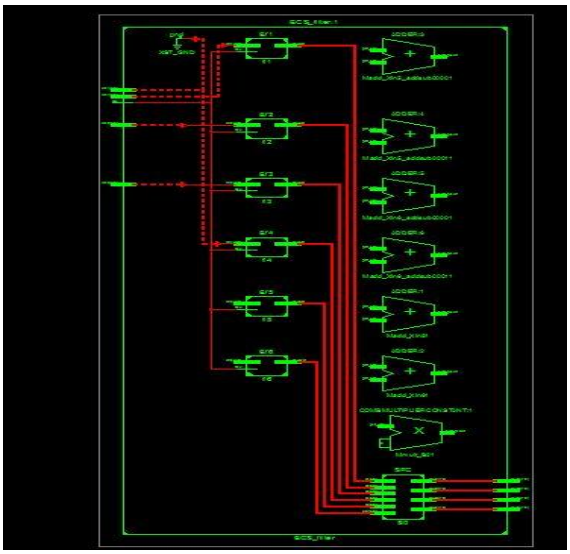

Fig6: RTL Schematic of Proposed scheme Using Xilinx ISE

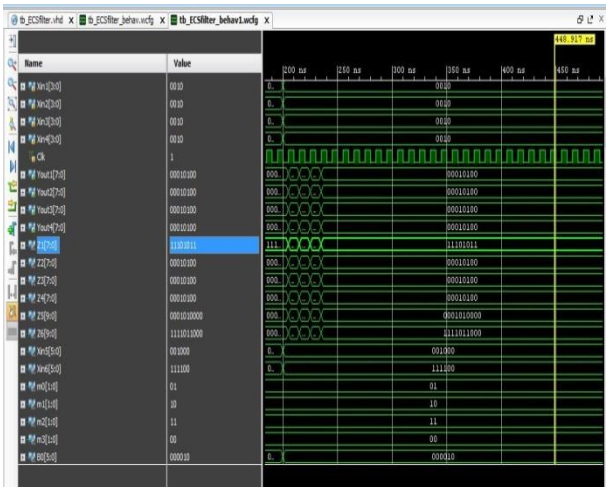

Fig 7: Behavioral Simulation of Parallel Filters with Fault Injected at Z1 Using Xilinx ISE.

7. CONCLUSION

A novel technique to execute fault tolerant parallel FIR digital filters has been proposed in this paper. The anticipated scheme manipulates the linearity of filters to implement an error correction method. Here inputs of two redundant filters which are linear combinations of the original filter inputs are used to detect and locate the errors. The previously proposed Technique was based on the use of Error Correction Codes (ECCs). This method considers each filter as a bit in the ECC. The proposed scheme beats the ECC technique (similar fault-tolerant capability with lower cost). Therefore, the proposed scheme can be useful to implement fault tolerant parallel filters.

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